

5 a discrete-time sampling circuit having a predetermined
6 sampling frequency, the discrete-time sampling circuit coupled to
7 the noise shaping network to generate an output signal with a lower
8 transition rate with respect to the predetermined sampling
9 frequency by a predetermined multiple.

1 8. The modulation stage of claim 1, wherein the sampling
2 circuit further comprises a logic circuit for suppressing sampling
3 of the input signal for a set number of clock cycles of a sampling
4 frequency clock.

a1 1 9. The modulation stage of claim 2, wherein the logic
2 circuit further comprises a transition detector for detecting a
3 transition in the output signal.

1 10. The modulation stage of claim 1, wherein the output
2 signal has a multi-state output, having at least three states.

1 11. A digital amplifier comprising:
2 a modulation stage for signal shaping; and
3 an H-bridge controller which generates a multi-state
4 output.

1 12. The digital amplifier of claim 5, wherein the H-bridge
2 controller a multi-state output, includes at least three states.

1 13. The digital amplifier of claim 6, wherein the H-bridge
2 controller has two output terminals, and the output signal on each
3 terminal is independently controlled.

1 14. A digital amplifier, comprising:

2 a summation circuit for summing an input signal with a
3 feedback signal, and generating a summed output signal;

4 a noise shaping network with an input coupled to the
5 output of the summation circuit and generating a noise shaped
6 signal;

7 a sampling stage with an input connected to the output of
8 the noise shaping network, and generating a sampled signal, the
9 sampling stage having a predetermined sampling frequency, and
10 generating an output signal with a lower transition rate with
11 respect to the sampling frequency by a predetermined multiple;

a 12 a feedback loop providing the output of the sampling
13 stage to the summation circuit and the noise shaping circuit; and

14 an output stage with inputs connected to the output of
15 the sampling stage and generating an output signal.

1 15. The digital amplifier of claim 8, wherein the output
2 stage includes an H-bridge controller.

1 16. The digital amplifier of claim 8, wherein the sampling
2 circuit further comprises a logic circuit for suppressing sampling
3 of the input signal for a set number of clock cycles of the
4 sampling frequency clock.

1 17. The digital amplifier of claim 10, wherein the logic
2 circuit further includes a transition detector for detecting a
3 transition in the output signal.

1 18. The digital amplifier of claim 8, wherein the output
2 signal of the sampling stage has a multi-state output, with at
3 least three states.

1 19. The digital amplifier of claim 8, wherein the noise
2 shaping network comprises a plurality of integrator stages.

1 20. A digital amplifier, comprising:
2 a summation circuit for summing an input signal with a
3 feedback signal, and generating a summed output signal;
4 a noise shaping network with an input coupled to the
5 output of the summation circuit and generating a noise shaped
6 signal;
7 a sampling stage with an input connected to the output of
8 the noise shaping network, and generating an output signal with a
9 multi-state output, with an least three states;
10 a feedback loop providing the output of the sampling
11 stage to the summation circuit and the noise shaping circuit; and
12 an output stage with inputs connected to the output of
13 the sampling stage and generating an output signal.

1 21. The digital amplifier of claim 14, wherein the output
2 stage includes an H-bridge controller.

1 22. The digital amplifier of claim 14, wherein the sampling
2 circuit generates an output signal with a lower transition rate
3 with respect to the sampling frequency by a predetermined multiple.

1 23. The digital amplifier of claim 14, wherein the sampling
2 circuit further comprises a logic circuit for suppressing sampling
3 of the input signal for a set number of clock cycles of the
4 sampling frequency clock.

1 24. The digital amplifier of claim 17, wherein the logic
2 circuit further comprises a transition detector for detecting a
3 transition in the output signal.